**IN THE SPECIFICATION**

Please amend paragraph [0042] of the specification as follows:

"The abstraction of the hardware components is illustrated in the following example. When a compiled version of service processor software architecture component 310A-B is executed on service processor [[100B]] 150, for example, service processor 150 may attempt to perform some task such as a diagnostic routine which may check the power status of client 120B. The request for the power status of client 120B may be presented to the HML. In one embodiment, the HML may interpret the request and determine which one or more ODs may be used to perform the task. The HML may use OD 320B, for example. OD 320B may invoke Accessor 350B. Accessor 350B may in turn create the transaction sequence necessary to read a 'power on' status bit such as bit 5 (not shown) within CSRs 380. This transaction sequence may then be handed back to the calling OD (e.g., OD 320B) to run at runtime. When run, the transactions in the sequence may be presented to hardware access layer 390, which may translate the transactions into commands for use by DMA engine 155 to create into DMA cycles. However, it is noted that there is no necessity that the particular client referenced in the call to the OD has the power status bit in it. For example, the power status bit may actually be implemented in a secondary IC located near client 120B. Thus, as described above, the OD can hide the details of where the power status actually resides in much the same way that the Accessors and Evaluators hide the details of the CSR."